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Description

[SCRIBE LINE STRUCTURE OF WAFER]

Cross Reference to Related Applications

[0001] This application claims the priority benefit of Taiwan application serial no. 92132504, filed on November 20, 2003.

Background of Invention

[0002] Field of the Invention

[0003] The present invention relates to a semiconductor wafer structure. More particularly, the present invention relates to a scribe line structure of wafer.

[0004] Description of the Related Art

[0005] Nowadays, integrated circuits (ICs) are used almost everywhere. However, the process of fabricating integrated circuits is complicated and involves four major stages: IC designs, wafer fabrication, wafer testing and wafer packaging. The total number of steps for fabricating an IC chip frequently exceeds a few hundreds and takes about a

month or two for the completion of all necessary steps.

[0006] At present, semiconductor devices are formed on monocrystalline silicon wafer. To lower production cost and to mass-produce chips, the diameter of a wafer has steadily increased from four inches to eight inches or more so that more chips can be fabricated on a single silicon wafer. The fabrication of integrated circuit devices can be roughly divided into three major stages, namely, silicon chip fabrication, integrated circuit fabrication and integrated circuit device packaging. In the integrated circuit fabrication stage, a number of patterns such as alignment marks, monitoring and/or measuring patterns, electrical testing patterns and product codes are formed on wafer scribe lines. Thereafter, the wafer is sawn to produce individual chip ready for carrying out the complicated integrated circuit packaging process.

[0007] However, various monitoring patterns on the scribe lines often subject the wafer chip on each side of the scribe lines to intense stress during the dicing process. As a result, chipping and delamination may appear close to the edges of the chip. Serious delamination is particularly likely to occur at the interface between a low dielectric constant material layer and another material layer because

the low dielectric constant material layer often has a poor adhesion with other dielectric material layer or metal layer.

Summary of Invention

[0008] Accordingly, at least one object of the present invention is to provide a wafer scribe line structure capable of reducing the amount of stress the wafer is subjected to during a dicing process.

[0009] At least a second object of this invention is to provide a wafer scribe line structure capable of preventing the growth of long chipping and the delamination of layers during a dicing process.

[0010] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a wafer scribe line structure. The wafer has a low dielectric constant material layer thereon. Furthermore, a plurality of lump patterns is formed in the low dielectric constant material layer within the scribe line. Each lump pattern is constructed using at least a metal layer or a metal plug. Moreover, the lump patterns form a cyclical staggered array that fills up the scribe line entirely.

[0011] This invention also provides an alternative wafer scribe

line structure. The scribe line on the wafer also incorporates a plurality of processing or testing patterns aside from a plurality of lump patterns embedded within a low dielectric constant material layer. Each lump pattern is constructed using at least a metal layer or a metal plug. Moreover, the lump patterns form a cyclical staggered array that fills up the scribe line entirely.

[0012] Since a plurality of lump patterns is formed within the low dielectric constant material layer of the scribe line in this invention, the amount of stress the wafer subjected to during the dicing process is greatly reduced. Hence, the probability of having a delamination at the interface between the low dielectric constant material layer and a nearby layer is also reduced.

[0013] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0014] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, to-

gether with the description, serve to explain the principles of the invention.

[0015] Fig. 1A is a top view of a wafer scribe line structure according to one preferred embodiment of this invention.

[0016] Fig. 1B is a magnified cross-sectional view along line A-A" in Fig. 1A.

[0017] Figs. 2A, 2B, 3A and 3B are schematic cross-sectional views showing a few examples for the scribe line structure according to this invention.

[0018] Fig. 4 is a top view of a wafer scribe line structure according to another preferred embodiment of this invention.

[0019] Fig. 5 is a top view of a wafer scribe line structure according to yet another embodiment of this invention.

Detailed Description

[0020] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0021] Fig. 1A is a top view of a wafer scribe line structure according to one preferred embodiment of this invention. Fig. 1B is a magnified cross-sectional view along line A-A"

in Fig. 1A. As shown in Figs. 1A and 1B, the wafer scribe line structure comprises a plurality of lump patterns 100 in a low dielectric constant material layer 104 within a scribe line 102. Furthermore, the lump patterns 100 form a cyclically staggered array that fills the scribe line 102 entirely so that the amount of stress the wafer subjected to during a dicing process is reduced. The width of each scribe line 102 is about 110μm, for example. The shape and size of all lump patterns 100 are identical, for example. The lump pattern 100 can have a variety of geometric shapes when viewing down from the top, and possible shapes for the lump patterns 100 include squares, rectangles, diamonds, triangles, circles, pentagons, hexagons or octagons. In this embodiment, an array of square lump patterns fills up the scribe line. In addition, the lump patterns 100 are formed in the low dielectric constant material layer 104 in the metal interconnect process simultaneously with the formation of metal layers or metal plugs, for example. In other words, each lump pattern 100 may be constructed from the attachment of a metal layer 106 to a metal plug 108. However, each lump pattern 100 may also be constructed from a metal plug 108 or a metal layer 106 alone as shown in Figs. 2A and 2B.

[0022] In this invention, there is no restriction on the way the metal layers 106 and the metal plugs 108 are joined together to form the lump patterns 100. Furthermore, the lump patterns 100 may be constructed using a multiple of metal layer 106/metal plug 108 sheets as shown in Figs. 3A and 3B. Moreover, the metal layer 106/metal plug 108 sheets are in direct contact with each other (as shown in Fig. 3A) or are interrupted by an intermediate layer (as shown in Fig. 3B).

[0023] In another embodiment of this invention, the wafer scribe line structure has processing or testing patterns aside from the lump patterned within the low dielectric constant material layer. In the following, a more detailed description of the embodiment is provided. However, since devices with identical labels to the aforementioned embodiment are fabricated using the same material and fabricating method, detailed description of such is omitted.

[0024] Fig. 4 is a top view of a wafer scribe line structure according to another preferred embodiment of this invention. As shown in Fig. 4, processing or testing patterns 110 and lump patterns 100 are formed within a scribe line 102. The patterns 110 are, for example, alignment marks, process-monitoring/measuring patterns, electrical testing

patterns or product identification marks. Furthermore, these marks are set up adjacent to the boundary of the scribe line 102 and occupied an area of $80 \times 70\mu m^2$, for example. In addition, the lump patterns 100 are set up within the low dielectric constant material layer in other parts of the scribe line 102. The lump patterns 100 are arranged to form a cyclically staggered array surrounding three sides of the patterns 110.

[0025] In another embodiment, the processing or testing patterns 110 may be set in the middle of the scribe line 102 so that the lump patterns 100 surround the patterns 110 on all four sides. Fig. 5 is a top view of a wafer scribe line structure according to yet another embodiment of this invention. As shown in Fig. 5, the lump patterns 100 are set up in regions outside the processing or testing patterns 110 within the scribe line 102. The lump patterns 100 are arranged to form a cyclically staggered array surrounding the patterns 110.

[0026] In summary, a plurality of cyclically staggered lump patterns is formed to cover the scribe line so that the amount of stress the wafer subjected to during a dicing process is greatly reduced. This prevents the growth of chipping near the cutting edges of a wafer chip and the delamina-

tion of the interface between the low dielectric constant material layer and a nearby layer. Furthermore, the lump patterns can be formed simultaneously with the metal interconnects in a metal interconnect fabrication process. Thus, the fabrication process is simplified and production yield is increased.

[0027] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.